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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/041,112	01/08/2002	Wipawan Yindeepol	100-22801	4475

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Mark C. Pickering
Law Offices of Mark C. Pickering
P.O. Box 300
Petaluma, CA 94953-0300

EXAMINER	
BAUMEISTER, BRADLEY W	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 12/03/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applicant(s)
10/041,112	Yindeepol et al.
Examiner	**Art Unit**
B. William Baumeister	2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Jun 23, 2003* .

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *25-59* is/are pending in the application.

4a) Of the above, claim(s) *33-38, 46-51, 55, and 59* is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *25-32, 39-45, 52-54, and 56-58* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☒ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☒ The proposed drawing correction filed on *Jun 25, 2003* is: a) ☐ approved b) ☒ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Election/Restriction

1. Applicants urge that claims 33-38, 46-51, 55 and 59--directed toward the non-elected embodiments of FIGs 5 and 6--should be rejoined because they respectively depend from allowable generic claims 25, 39, 52 and 56. However, this argument is not persuasive because these generic, independent claims stand rejected for the reasons set forth hereinbelow. Accordingly, claims 33-38, 46-51, 55 and 59 are withdrawn from prosecution as being directed towards non-elected inventions.

Drawings

2. The corrected or substitute drawings were received on 7/22/2003 (paper #9). These drawings are not approved.

a. FIG 7 still includes the label "NXB," but this terminology has been removed from the specification by the last amendment.

b. FIG 7 includes the label "N sink," but the specification recites an "N+ sinker" (e.g., page 8 of the specification (see page 7 of the amendment, line 4).

c. Unlike FIG 7, Figs 5 and 6 depict (using the reference numerals of FIG 5) the vertical lines associated with the interior of trench isolation elements 53 extending downward through n-region 52 so as to terminate at the top of NBL 50, and thereby producing two unlabeled squares that are bounded by the trench 53, the n-region 52 and the NBL 50. It is

unclear whether these lines are spurious drafting errors, or alternatively are intended to indicate that the n-region 52 may be further doped to a higher concentration than the unlabeled square regions (which is not supported by the written specification).

d. Appropriate correction or explanation of these and any other inconsistencies is required.

Specification

3. The specification inconsistently recites the sinker (e.g., FIG 5, element 52) is doped N+ (see e.g., page 4 of the amendment filed 11/6/2003, page 4, line 6) and doped N (see e.g., page 5 of the amendment, fourth line from bottom). Applicant should review and edit the entire specification for consistency.

4. The specification has been amended to recite that the dopant concentrations of the first conductor and the third region may be substantially equal (see e.g., amendment filed 11/6/2003, page 3, fourth full paragraph, last sentence). The specification as originally filed did not disclose that the dopant concentrations of the first conductor and the third region may be substantially equal. Rather, the originally-filed specification states that the layer over the NBL (i.e., layer 50 of FIG 5, layer 114 of FIG 6 or layer 250 of FIG 7) may be an N-epi or N+ sinker layer, thereby indicating that this layer may be either a moderately (or lightly?) Doped epi-layer, or alternatively, a heavily doped sinker or tub. But the original specification further states e.g., in relation to the FIG 5 embodiment, "A second portion 68 of the first polysilicon layer 54 is n-doped to define a

n-extrinsic base (NXB) 70 in the n-epitaxial or n+ sinker region 52. (Original specification, page 7, lines 5-6). This passage alternatively implies that even if an N+ sinker is employed, the n-type polysilicon line 68 will still be more heavily doped, because if these two regions were doped to substantially the same level, the subsequent processing would not produce an autodoped region 70 (a region that is effectively higher in dopant concentration than that of the N+ sinker).

Claim Rejections - 35 USC § 112

5. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claims 39-51 and 56-59 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claim 39 and similarly worded claim 56--from which all of these other claims ultimately depend--recites:

> ... the first region including a third region that lies vertically below all of the second region, has the first conductivity type, and has a substantially uniform dopant concentration, and
>
> a first conductor..., *the dopant concentration of the third region and the dopant concentration of the first conductor being substantially equal*;... (italics added)

The specification as originally filed did not disclose that the dopant concentrations of the first conductor and the third region may be substantially equal. Rather, the originally-filed specification states that the layer over the NBL (i.e., layer 50 of FIG 5, layer 114 of FIG 6 or layer 250 of FIG 7) may be an N-epi or N+ sinker layer, thereby indicating that this layer may be either a moderately (or lightly?) Doped epi-layer, or alternatively, a heavily doped sinker or tub. But the original specification further states e.g., in relation to the FIG 5 embodiment, "A second portion 68 of the first polysilicon layer 54 is n-doped to define a n-extrinsic base (NXB) 70 in the n-epitaxial or n+ sinker region 52. (Original specification, page 7, lines 5-6). This passage alternatively implies that even if an N+ sinker is employed, the n-type polysilicon line 68 will still be more heavily doped, because if these two regions were doped to substantially the same level, the subsequent processing would not produce an autodoped region 70 (a region that is effectively higher in dopant concentration than that of the N+ sinker).

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 39-51 and 56-59 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

a. In the following limitation of claims 39 and the similar limitation of claim 56, "the dopant concentration of the third region and the dopant concentration of the first conductor being substantially equal;" the term "substantially" is a relative term which renders the claim indefinite. The term "substantially " is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. For example, it is unclear whether "substantially" is intended to mean that (1) the respective elements both have the same general concentrations, such as both being N+ (e.g., ~1e18-1e21) or both being n type (e.g., ~1e17-1e19); or alternatively that (2) further within these broad ranges of potential doping concentrations (e.g., N+ or N), both elements have more specific concentrations that are substantially equal (e.g., both about 1e19).

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. Claim 25 is rejected under 35 U.S.C. 102(b) as being anticipated by Castrucci et al. 516.

a. Castrucci discloses, see e.g., FIG 4, a buried N+ layer 46; an N epi region 50 formed on the buried region; the N epi region 50 including (1) a first N region that extends from

the N+ subcollector to the surface and includes N+ well 40, and (2) a second, contiguous P region 38 that contacts the surface and the first region, wherein no n-type regions are enclosed within P region 38; a first conductor (either metal layer 36 or 32) formed on the surface to make an electrical connection with the first region; and a second conductor 34, formed on the surface and spaced apart from the first conductor.

b. WL 36 reads on the first conductor because (1) the claim does not require that the portion of the epi-surface with which the first conductor makes contact be part of the first region (assuming P region 42 is deemed to not be part of the first region); rather, the claim only requires that the first conductor make "electrical connection with the first region," which WL 36 does.

c. Alternatively, "free metal" layer 32--which is not electrically connected to any further structure--reads on the first conductor because the metal layer 32 is in structural contact with N+ region 40 and therefore makes electrical connection therewith.

Claim Rejections - 35 USC § 103

11. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

12. Claims 25-32 and 52-54 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ibi et al. '766 in view of Cervin-Lawry et al. '722 and Castrucci '516.

a. Ibi teaches conventional zener-zap diodes (see e.g., FIGs 1 and 2) wherein spaced-apart p and n regions 13/14 are formed in a p type well 12. Metal lines 15 are formed over the n and p regions so that a reverse breakdown voltage can be applied therebetween for adjusting the circuit resistance. The insulating regions 16-1 and 16-2 may be composed of either SiO2 or SiN (col. 2, lines 61-) and the p and n dopant types may be reversed so that the tub 12 is n-doped (col. 4, lines 43-). Ibi does not disclose that silicided poly lines may be alternatively employed for the metal lines 15. Ibi discloses that P-region 12 is formed as a well (or sinker) as opposed to as an epi layer. Ibi also does not disclose a buried layer having the same conductivity type as that of the epi-layer's first region.

b. Regarding the issue of metal vs. silicided poly, Cervin teaches that zener-zap antifuses that employ silicided 136/138 poly lines 118/120 that connect to respective p and n regions of a semiconductor substrate so that a reverse-bias can be employed there across to cause a silicide filament to extend fully between the poly lines to create a short or bridge. Cobalt may be employed as the refractory metal silicide (col. 4, line 52). Conductivity types may be reversed (col. 7, line 31-). The silicided lines may be employed in single or double poly processes (col. 7, line 18). It would have been obvious to one of ordinary skill in the art at the time of the invention to have employed the silicided poly lines as taught by Cervin in the Ibi zap diode for the purpose of providing an anti fuse structure requiring a relatively lower programming voltage than afforded by metal interconnects as taught by Cervin (see e.g., BACKGROUND and the discussion of the prior art at col. 3-).

c. Regarding the issues of (i) the well vs. the epi-layer and (ii) the buried layer, Castrucci teaches Zener diode structures, as was explained above, and further teaches that a buried layer 46 having the same conductivity type as that of the overlying epi-layer 50 may also be employed.

i. It would have been obvious to one of ordinary skill in the art at the time of the invention to have formed the p-well of Ibi/Cervin-Lawry instead as an epi-layer as taught by Castrucci, because these were conventionally-known functionally-equivalent structures, each with respective, but well understood, advantages: e.g., relative to doped wells, epi-layers generally produce higher carrier mobilities but have higher manufacturing costs.

ii. It would have been obvious to one of ordinary skill in the art at the time of the invention to have further included within a Zener diode structure produced according to Ibi/Cervin-Lawry, such a buried layer as taught by Castrucci, for the purpose of improving the device characteristics (see e.g., Castrucci, col. 4, lines 1-4).

d. Regarding claims 31 and 32, Cervin teaches that it was known to employ a double poly processes so as to cause one of the two poly lines to vertically overlie and be isolated from the first conductor. It would have been obvious to one of ordinary skill in the art at the time of the invention to have formed the silicided zener zap diode structure of Ibi/Cervin as explained above through the use of a conventional double poly process such that the poly lines vertically overlap as taught by Cervin for the purpose of reducing and better controlling the lateral spacing

of the p and n contact regions relative to a structure obtained by a lithographic process, thereby further reducing the voltage requirements as taught by Cervin (e.g., col. 4, lines 1-29).

e. In further regard to claim 31, which requires that one end of the second conductor be substantially higher than the first end, while Cervin-Lawry teaches that the overlying emitter conductor 120 alternatively has both of its ends substantially higher than the central portion, this is because the specific structure of Cervin-Lawry is employed in a BJT-like construction wherein the first conductor 118 extends around the opening through which the second conductor 120 makes contact with the semiconductor surface. Nonetheless, it would have been obvious to the skilled artisan who is modifying Ibi so as to include the double-poly process taught by Cervin-Lawry for the reasons set forth above, to form the second conductor 15-2 so as to have only one end extending above the first conductor 15-1 (and therefore have one end be substantially higher than the other) because unlike Cervin-Lawry, Ibi teaches that the first conductor 15-1 does not extend around the contact hole associated with second conductor 15-2; but rather, extends adjacent to one side of the second contact hole.

13. Claims 25-32 and 52-54 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dark et al. '189 in view of Cervin-Lawry et al. '722 and Castrucci '516.

a. Dark '189 discloses and claims conventional zener-zap diodes (see e.g., FIGs 1A-1F) wherein spaced-apart p and n regions 107a/b are formed in a common doped region 104, which in turn, may be doped either p-type or n-type. P-type and N-type poly lines 108a/b are

formed over the p and n regions so that a reverse breakdown voltage can be applied therebetween for adjusting the circuit resistance. The poly lines may be silicided. (e.g., col. 2, lines 36-38). Regarding those claims that so require, Dark does not disclose that it is the silicide metal which forms the conductive path, but rather that it is the metal (e.g., Al) of the overlying contacts that makes the conductive path. Dark discloses that common doped region 104 is formed as a well (or sinker) as opposed to as an epi layer. Dark also does not disclose a buried layer having the same conductivity type as that of the epi-layer's first region.

b. Regarding the issue of metal vs. silicided poly, Cervin teaches that zener-zap antifuses that employ silicided 136/138 poly lines 118/120 that connect to respective p and n regions of a semiconductor substrate so that a reverse-bias can be employed there across to cause a silicide filament to extend fully between the poly lines to create a short or bridge. Cobalt may be employed as the refractory metal silicide (col. 4, line 52). Conductivity types may be reversed (col. 7, line 31-). The silicided lines may be employed in single or double poly processes (col. 7, line 18). It would have been obvious to one of ordinary skill in the art at the time of the invention to have employed the silicided poly lines as taught by Cervin in the Dark zap diode for the purpose of providing an anti fuse structure requiring a relatively lower programming voltage than afforded by metal interconnects as taught by Cervin (see e.g., BACKGROUND and the discussion of the prior art at col. 3 -).

c. Regarding the issues of (i) the well vs. the epi-layer and (ii) the buried layer, Castrucci teaches Zener diode structures, as was explained above, and further teaches that a

buried layer 46 having the same conductivity type as that of the overlying epi-layer 50 may also be employed.

i. It would have been obvious to one of ordinary skill in the art at the time of the invention to have formed the p-well of Dark/Cervin-Lawry instead as an epi-layer as taught by Castrucci, because these were conventionally-known functionally-equivalent structures, each with respective, but well understood, advantages: e.g., relative to doped wells, epi-layers generally produce higher carrier mobilities but have higher manufacturing costs.

ii. It would have been obvious to one of ordinary skill in the art at the time of the invention to have further included within a Zener diode structure produced according to Dark/Cervin-Lawry, such a buried layer as taught by Castrucci, for the purpose of improving the device characteristics (see e.g., Castrucci, col. 4, lines 1-4).

d. Regarding claims 31 and 32, Cervin teaches that it was known to employ a double poly processes so as to cause one of the two poly lines to vertically overlie and be isolated from the first conductor. It would have been obvious to one of ordinary skill in the art at the time of the invention to have formed the silicided zener zap diode structure of Dark/Cervin as explained above through the use of a conventional double poly process such that the poly lines vertically overlap as taught by Cervin for the purpose of reducing and better controlling the lateral spacing of the p and n contact regions relative to a structure obtained by a lithographic process, thereby further reducing the voltage requirements as taught by Cervin (e.g., col. 4, lines 1-29).

e. In further regard to claim 31, which requires that one end of the second conductor be substantially higher than the first end, while Cervin-Lawry teaches that the overlying emitter conductor 120 alternatively has both of its ends substantially higher than the central portion, this is because the specific structure of Cervin-Lawry is employed in a BJT-like construction wherein the first conductor 118 extends around the opening through which the second conductor 120 makes contact with the semiconductor surface. Nonetheless, it would have been obvious to the skilled artisan who is modifying Dark so as to include the double-poly process taught by Cervin-Lawry for the reasons set forth above, to form the second conductor so as to have only one end extending above the first conductor (and therefore have one end be substantially higher than the other) because unlike Cervin-Lawry, Dark teaches that the first conductor does not extend around the contact hole associated with second conductor; but rather, extends adjacent to one side of the second contact hole. Further, Dark expressly states that each poly conductor extends up onto field oxide 102 to reduce subsequent metallization step coverage requirements, although this may not be required in all applications. (col. 2, lines 33-36)

Double Patenting

14. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed.

Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

15. Claims 25-32 and 52-54 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-10 of U.S. Patent No. 6,563,189 issued to Dark et al. in view of Cervin-Lawry '722 and Castrucci '516, as applied to the claims in the rejections above for the bases and reasons set forth therein.

Response to Arguments

16. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

17. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Li et al. '387 (see e.g., FIG 5B).

INFORMATION ON HOW TO CONTACT THE USPTO

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to the examiner, **B. William Baumeister,** at **(703) 306-9165.** The examiner can normally be reached Monday through Friday, 8:30 a.m. to 5:00 p.m. If the Examiner is not available, the Examiner's supervisor, Mr. Tom Thomas, can be reached at (703) 308-2772. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

B. William Baumeister

Primary Examiner, Art Unit 2815

11/29, 2003

BRADLEY BAUMEISTER
PRIMARY EXAMINER